Appl. No. 10/502,422 Amdt. Dated July 20, 2007 Reply to Office action of April 20, 2007 Attorney Docket No. P16178-US1 FUS/LIP/07-1178

REMARKS/ARGUMENTS

1.) Withdrawal of Prior Rejections

The Applicant thanks the Examiner for his consideration of Applicant's prior arguments, traversing the rejection of the claims as anticipated by Doblar, *et al.* (U.S. Patent No. 6,194,969), and the Examiner's acceptance of those arguments as persuasive and withdrawal of the rejections based thereon.

Claim Rejections – 35 U.S.C. §103(a)

In the present Office Action, the Examiner has rejected claims 11, 12, 16, 17 as being unpatentable over Tamura (US 2003/0042957) in view of Doblar; and rejected claims 13-15 as being unpatentable over Tamura in view of Doblar and further in view of Mosley, *et al.* (United States Patent No. 6,597,197). The Applicant traverses the rejections.

Claim 11

Claim 11 recites:

A computer system clocking system, said system comprising:

at least two units with clock functionality, the units being coupled to a common system clock line, a common internal clock line, and a logic bus, wherein one unit is dedicated as a master unit at a time, the dedication of the master unit being dependent on at least a signal being given so as not to select a given unit for being a master unit, and if a given unit is dedicated as master unit when such a signal is given, the system performing a switchover causing another unit as the one not selected to be dedicated as master unit, each unit comprising:

a clock source for generating a clock source signal, the clock source signal being adapted for being output on the internal clock line; and a phase lock loop device generating a signal, which is derived from the signal on the internal clock line, and which is output on the system clock line if the unit is dedicated as master unit, wherein one source clock signal of a unit is output on the internal clock line and all phase lock loop devices of all units generate phase lock loop output signals derived from the internal clock signal, the outputs of the phase lock loop devices being in phase with one another such that switchover from one phase lock loop output signal to another is seamless. (emphasis added).

Appl. No. 10/502,422 Amdt. Dated July 20, 2007 Reply to Office action of April 20, 2007 Attorney Docket No. P16178-US1 EUS/JIP/07-1178

First, the Examiner asserts that Tamura discloses certain limitations of claim 11. but states that "Tamura fails to disclose the following limitations." with respect to which he then refers to the teachings of Doblar. The limitations the Examiner asserts as taught by Tamura are the very few limitations italicized in claim 11, supra, while all of the other limitations of claim 11, which are underlined, are asserted by the Examiner as being disclosed by Doblar. The few limitations for which the Examiner relies on the teachings of Tamura, however, are essential limitations for which the remaining claim elements depend. For example, later claim limitations, for which the Examiner looks to the teachings of Doblar, specifically depend on the "at least two units with clock functionality, the units being coupled to a common system clock line," and "a common internal clock line" limitations. Thus, if Doblar did in fact teach the limitations which the Examiner asserts, it would necessarily need to teach the limitations for which the Examiner relies on the teachings of Tamura. But Doblar does not teach such limitations. which was the basis of Applicant's prior arguments traversing the Examiner rejection of the claims solely in view of Doblar, which arguments the Examiner states in the present Office Action were "persuasive." This fact was supported in Applicant's prior arguments. wherein Applicant stated that:

"Doblar does not disclose a <u>common</u> system clock line nor a <u>common</u> internal clock line. According to Doblar, clock signals from fan-out buffers 208A/B are individually provided to phase detector inputs of other devices, but no two units (105A, 105B) share a clock line; *i.e.*, no two units are hooked up on the same common clock line."

Second, as also noted in Applicant's prior arguments, the Examiner equates a phase lock loop device with Figure 3 of Doblar. Claim 11, however, states that each unit has a phase lock loop device. If Figure 3 of Doblar constitutes a phase lock loop device, it should be found in each unit, which is apparently not taught by Doblar – i.e., only one Figure 3 device is expressly taught by Doblar. Giving the broadest possible scope to the Examiner's reading of Doblar, however, it might be assumed that the clock board 105B constitutes a PLL of one unit, while Figure 3 constitutes a PLL of another unit. According to Applicants' invention recited in claim 11, however, the PLL (e.g., 105B) of each unit should generate a signal which is derived form the signal on the internal clock

Appl. No. 10/502,422 Amdt. Dated July 20, 2007 Reply to Office action of April 20, 2007 Attorney Docket No. P16178-US1 EUS/JJP/07-1178

line (e.g., 208C). That, however, is not the case according to Dobblar. Furthermore, according to claim 11, the PLL signal is output on the system clock line (e.g., 106A), which is also not taught by Doblar. Therefore, even assuming a broad scope of the Examiner's reading of Doblar, Doblar fails to teach the limitations of claim 11 stated by the Examiner

Finally, it is noted that <u>all</u> of the claim limitations for which the Examiner now relies on the teachings of Tamura are the claim limitations which the Applicant asserted in response to the prior Office Action were not disclosed by Doblar, which the Examiner previously relied on as anticipating the claims. The Examiner has now merely looked for the disclosure of such limitations in Tamura, without any regard for the cooperation between claim elements, much less any suggestion in either of Doblar or Tamura to combine their teachings. The Examiner <u>provides no support for the conclusory statement of obviousness</u>; the Examiner merely states that, "taking the combined teachings of Tamura, Doblar as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of [the limitations asserted by the Examiner to be disclosed by Doblar] into Tamura to allow a phase-aligned slave clock to replace a master clock upon failure of the master clock." The Examiner, however, provides to motivation for such combination. As stated in MPEP §706.02(j):

The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985).

* * :

It is important for an examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply. (emphasis added) Appl. No. 10/502,422 Amdt. Dated July 20, 2007 Reply to Office action of April 20, 2007 Attorney Docket No. P16178-US1 EUS/J/P/07-1178

Whereas the Examiner has not provided any reasoning as to why one of ordinary skill in the art would have found the claimed invention obvious, the Examiner has failed to establish a prima facie case of obviousness of claim 11.

Claim 13

With respect to the Examiner's rejection of claim 13, it is noted that the Examiner previously rejected that claim as anticipated by Doblar. In traversing that rejection, the Applicant directed his arguments to the fact that Doblar failed to teach the claim limitations relating to a "bidirectional port." Having accepted Applicant's arguments as "persuasive," the Examiner now raises an obviousness rejection of that claim by simply pointing to a bidirectional port in the teachings of Mosley. As with the Examiner's obviousness rejection of claim 11, the Examiner has now merely looked for the disclosure of such limitations in Mosley, without any regard for the cooperation between claim elements, much less any suggestion in either of Doblar or Tamura to combine their teachings with the teachings of Mosley. Again, the Examiner provides no support for the conclusory statement of obviousness.

For the forgoing reasons, the Examiner has not established a *prima facie* case of obviousness of claims 11 or 13. Furthermore, whereas claims 12-17 are dependent from claim 11, and claims 14-15 are also dependent from claim 13, and include the limitations thereof, those claims are also not obvious over Tamura in view of Doblar and/or Mosley.

* * *

Appl. No. 10/502,422 Amdt. Dated July 20, 2007 Reply to Office action of April 20, 2007 Attorney Docket No. P16178-US1 EUS/JIP/07-1178

CONCLUSION

In view of the foregoing remarks, the Applicant believes all of the claims currently pending in the Application to be in a condition for allowance. The Applicant, therefore, respectfully requests that the Examiner withdraw all rejections and issue a Notice of Allowance for claims 11-17.

<u>The Applicant requests a telephonic interview</u> if the Examiner has any questions or requires any additional information that would further or expedite the prosecution of the Application.

Respectfully submitted.

/Roger S. Burleigh, Reg#40542/

Roger S. Burleigh Registration No. 40.542

Date: July 20, 2007

Ericsson Inc. 6300 Legacy Drive, M/S EVR 1-C-11 Plano. Texas 75024

(972) 583-5799 roger.burleigh@ericsson.com